ESP32-S2-WROVER
ESP32-S2-WROVER-I

Datasheet

2.4 GHz Wi-Fi (802.11 b/g/n) module

Built around ESP32-S2 series of SoC (chip revision 0), Xtensa® single-core 32-bit LX7 microprocessor

Flash up to 16 MB, 2 MB PSRAM

37 GPIOs, rich set of peripherals

On-board PCB antenna or external antenna connector

ESP32-S2-WROVER

ESP32-S2-WROVER-I

Version1.2

Espressif Systems

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://www.espressif.com/documentation/esp32-s2-wrover_esp32-s2-wrover-i_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-S2 embedded, Xtensa® single-core 32-bit LX7 microprocessor, up to 240 MHz
- 128 KB ROM
- 320 KB SRAM
- 16 KB SRAM in RTC

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Operating frequency: 2412 ~ 2484 MHz

Peripherals

- GPIO, SPI, LCD, UART, I2C, I2S, Camera interface, IR, pulse counter, LED PWM, TWAI® (compatible with ISO 11898-1, i.e. CAN Specification 2.0), full-speed USB OTG, ADC, DAC, touch sensor, temperature sensor

Integrated Components on Module

- 40 MHz crystal oscillator
- 4 MB SPI flash
- 2 MB PSRAM

Antenna Options

- On-board PCB antenna (ESP32-S2-WROVER)
- External antenna via a connector (ESP32-S2-WROVER-I)

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: –40 ~ 85 °C

Certification

- RF certification: See certificates for ESP32-S2-WROVER and ESP32-S2-WROVER-I
- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD

1.2 Description

ESP32-S2-WROVER and ESP32-S2-WROVER-I are two powerful, generic Wi-Fi MCU modules that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios related to Internet of Things (IoT), such as embedded systems, smart home, wearable electronics, etc.

ESP32-S2-WROVER comes with a PCB antenna (ANT). ESP32-S2-WROVER-I comes with a connector for an external antenna (CONN).

They both feature a 4 MB external SPI flash and an additional 2 MB SPI Pseudo static RAM (PSRAM). The information in this datasheet is applicable to both modules.

The ordering information for the two modules is as follows:

Table 1: Ordering Information

Module	Chip Embedded	Flash	PSRAM	Module Dimensions (mm)
ESP32-S2-WROVER (ANT)	ESP32-S2	4 MB	2 MB	18.0 × 31.0 × 3.3
ESP32-S2-WROVER-I (CONN)				

[1] These modules can be shipped with different flash sizes.

At the core of the modules is ESP32-S2 *, an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. You can power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds.

ESP32-S2 integrates a rich set of peripherals including SPI, I2S, UART, I2C, LED PWM, TWAI® controller, ADC, DAC, touch sensor, temperature sensor, as well as up to 43 GPIOs. It also includes a full-speed USB OTG (OTG) interface to enable USB communication.

Note:
* For more information on ESP32-S2, please refer to *ESP32-S2 Series Datasheet*.

1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Home Control Panel
- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications
- Smart POS Machines

Contents

List of Tables

List of Figures

2 Block Diagram

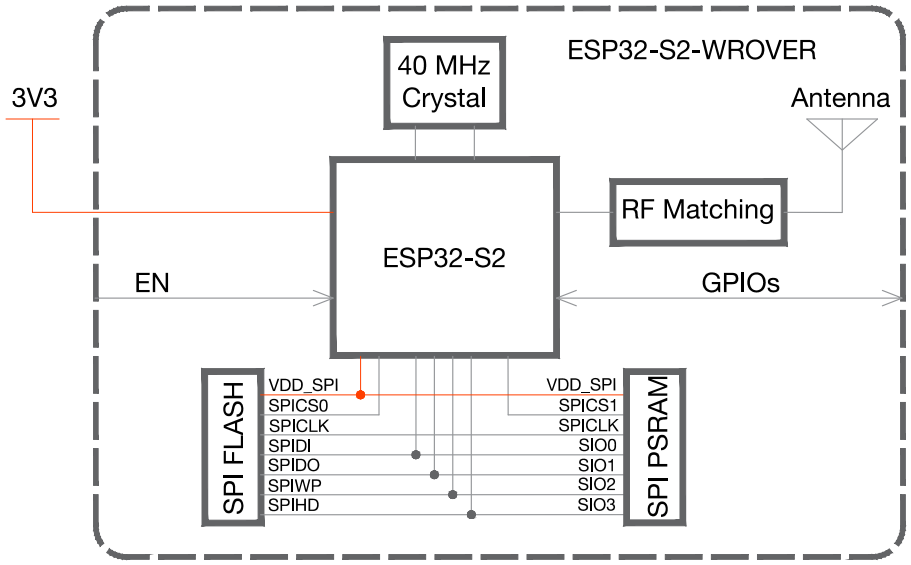

Figure 1: ESP32-S2-WROVER Block Diagram

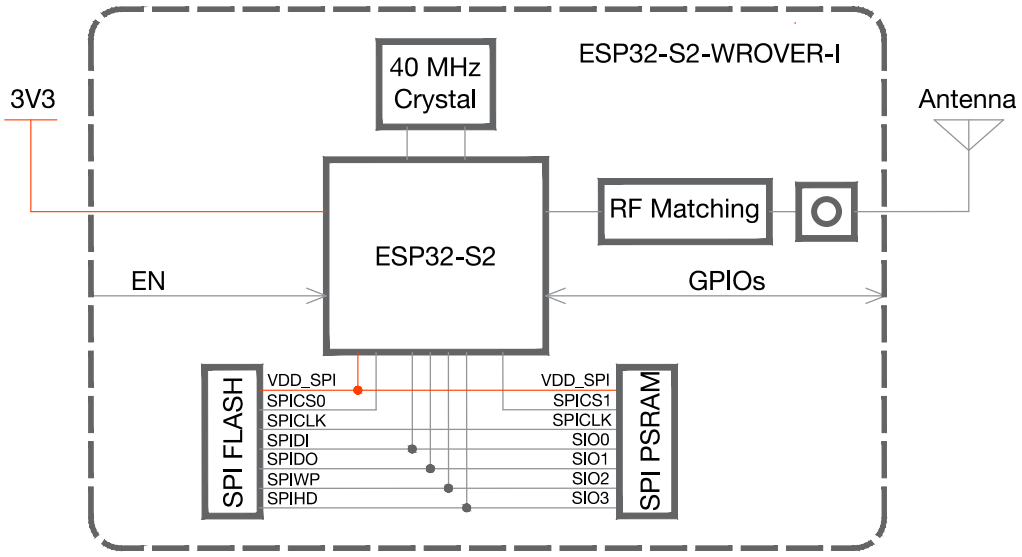

Figure 2: ESP32-S2-WROVER-I Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 7.1 *Physical Dimensions*.

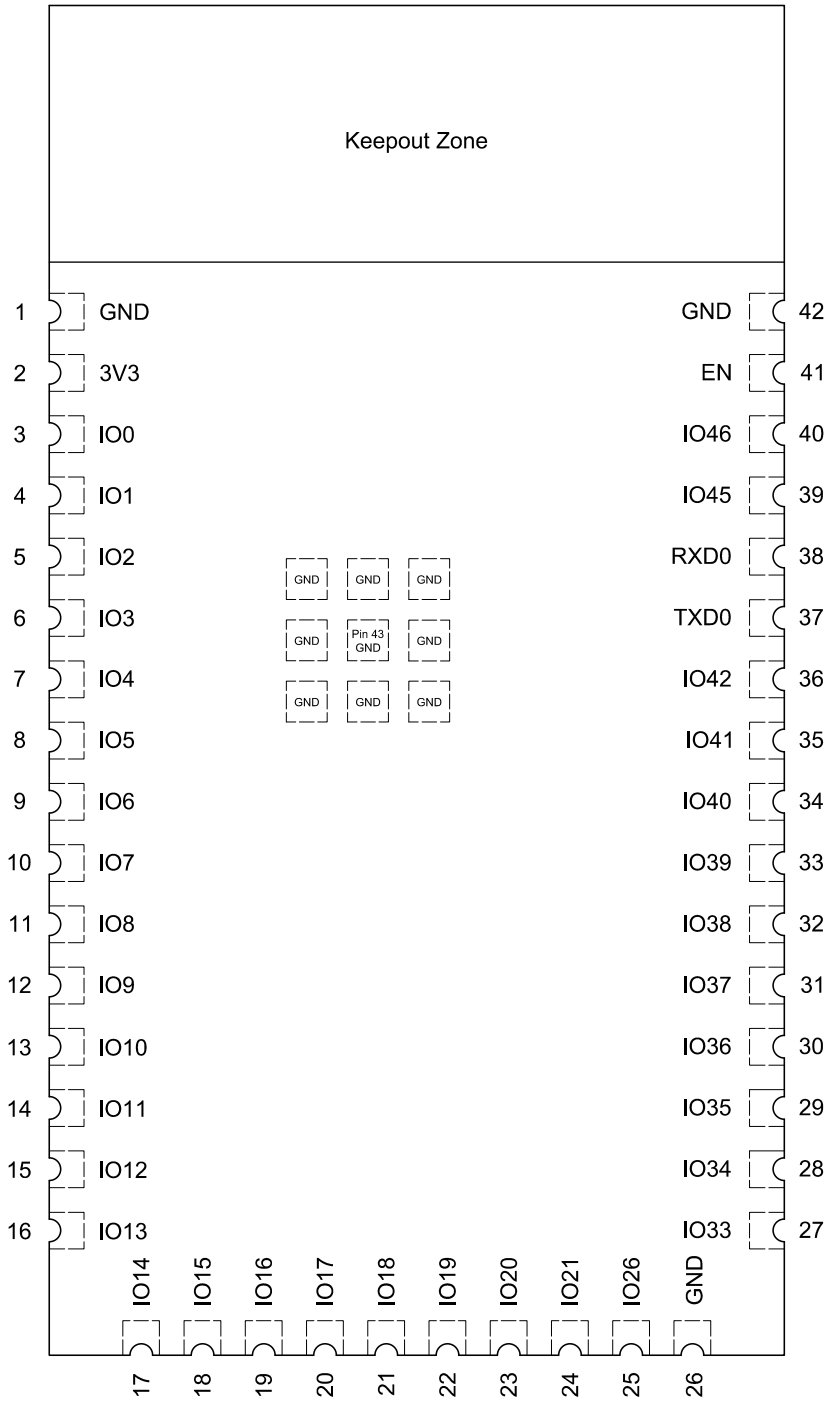

Figure 3: Pin Layout (Top View)

3.2 Pin Description

The module has 42 pins. See pin definitions in Table 2.

For peripheral pin configurations, please refer to *ESP32-S2 Series Datasheet*.

Table 2: Pin Definitions

Name	No.	Type[1]	Function
GND	1	P	Ground
3V3	2	P	Power supply
IO0	3	I/O/T	RTC_GPIO0, GPIO0
IO1	4	I/O/T	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
IO2	5	I/O/T	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
IO3	6	I/O/T	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
IO4	7	I/O/T	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
IO5	8	I/O/T	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
IO6	9	I/O/T	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
IO7	10	I/O/T	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
IO8	11	I/O/T	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
IO9	12	I/O/T	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD
IO10	13	I/O/T	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4
IO11	14	I/O/T	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5
IO12	15	I/O/T	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6
IO13	16	I/O/T	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7
IO14	17	I/O/T	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS
IO15	18	I/O/T	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	19	I/O/T	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	20	I/O/T	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
IO18	21	I/O/T	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
IO19	22	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
IO20	23	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
IO21	24	I/O/T	RTC_GPIO21, GPIO21
IO26	25	I/O/T	SPICS1, GPIO26 [2]
GND	26	P	Ground
IO33	27	I/O/T	SPIIO4, GPIO33, FSPIHD
IO34	28	I/O/T	SPIIO5, GPIO34, FSPICS0
IO35	29	I/O/T	SPIIO6, GPIO35, FSPID
IO36	30	I/O/T	SPIIO7, GPIO36, FSPICLK
IO37	31	I/O/T	SPIDQS, GPIO37, FSPIQ
IO38	32	I/O/T	GPIO38, FSPIWP
IO39	33	I/O/T	MTCK, GPIO39, CLK_OUT3
IO40	34	I/O/T	MTDO, GPIO40, CLK_OUT2
IO41	35	I/O/T	MTDI, GPIO41, CLK_OUT1
IO42	36	I/O/T	MTMS, GPIO42
TXD0	37	I/O/T	U0TXD, GPIO43, CLK_OUT1

Cont'd on next page

Table 2 – cont'd from previous page

Name	No.	Type[1]	Function
RXD0	38	I/O/T	U0RXD, GPIO44, CLK_OUT2
IO45	39	I/O/T	GPIO45
IO46	40	I	GPIO46
EN	41	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
GND	42	P	Ground

[1] P: power supply; I: input; O: output; T: high impedance.

[2] By default, IO26 is connected to the CS pin of the PSRAM and cannot be used for other functions.

3.3 Strapping Pins

Note:

The content below is excerpted from Section Strapping Pins in *ESP32-S2 Series Datasheet*. For the strapping pin mapping between the chip and modules, please refer to Chapter 5 *Module Schematics*.

ESP32-S2 has three strapping pins:

- GPIO0
- GPIO45
- GPIO46

Software can read the values of corresponding bits from register "GPIO_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to the chip's internal weak pull-up/pull-down during the chip reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S2.

After reset, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration of the strapping pins.

Table 3: Strapping Pins

VDD_SPI Voltage [1] [2]			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Booting Mode [3]			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0

GPIO46	Pull-down	Don't-care	0
Enabling/Disabling ROM Messages Print During Booting [4] [5]			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See note 5	See note 5

Note:

1. The functionality of strapping pin GPIO45 to select VDD_SPI voltage may be disabled by setting VDD_SPI_FORCE eFuse to 1. In such a case the voltage is selected with eFuse bit VDD_SPI_TIEH.
2. Since ESP32-S2FH2, ESP32-S2FH4, ESP32-S2FN4R2, and ESP32-S2R2 come with both/either 3.3 V SPI flash and/or PSRAM, VDD_SPI must be configured to 3.3 V.
3. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
4. ROM code can be printed over U0TXD (by default) or DAC_1, depending on the eFuse bit.
5. When eFuse UART_PRINT_CONTROL value is:
   0, print is normal during boot and not controlled by GPIO46.
   1 and GPIO46 is 0, print is normal during boot; but if GPIO46 is 1, print is disabled.
   2 and GPIO46 is 0, print is disabled; but if GPIO46 is 1, print is normal.
   3, print is disabled and not controlled by GPIO46.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	85	°C

4.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	–40	—	85	°C

4.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL_nRST}	Chip reset voltage	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

4.4 Current Consumption Characteristics

Owing to the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *RTC and Low-Power Management* in *ESP32-S2 Series Datasheet*.

Table 7: Current Consumption Depending on RF Modes

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	310
		802.11g, 20 MHz, 54 Mbps, @15 dBm	220
		802.11n, 20 MHz, MCS7, @13.5 dBm	200
		802.11n, 40 MHz, MCS7, @13.5 dBm	160
	RX [2]	802.11b/g/n, 20 MHz	63
		802.11n, 40 MHz	68

[1] The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on 100% duty cycle.

[2] The current consumption figures in RX mode are for cases where the peripherals are disabled and the CPU idle.

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-S2 Series Datasheet*.

The measurements below are applicable to ESP32-S2, ESP32-S2FH2, and ESP32-S2FH4. Since ESP32-S2FN4R2 and ESP32-S2R2 are embedded with PSRAM, their current consumption might be higher.

Table 8: Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ	
			All Peripherals Clocks Disabled (mA)	All Peripherals Clocks Enabled (mA)[1]
Modem-sleep[2,3]	240	CPU is idle	20.0	28.0
		CPU is running	23.0	32.0
	160	CPU is idle	14.0	21.0
		CPU is running	16.0	24.0
	80	CPU is idle	10.5	18.4
		CPU is running	12.0	20.0

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem sleep mode, Wi-Fi is clock gated.

[3] In Modem-sleep mode, the consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 9: Current Consumption in Low-Power Modes

Mode	Description		Typ (μA)
Light-sleep[1]	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance		750
Deep-sleep	The ULP co-processor is powered on[2]	ULP-FSM	170
		ULP-RISC-V	190
	ULP sensor-monitored pattern[3]		22
	RTC timer + RTC memory		25
	RTC timer only		20
Power off	CHIP_PU is set to low level, the chip is powered off		1

[1] In Light-sleep mode, with all related SPI pins pulled up, the current consumption of the embedded PSRAM is 140 μA. Chip variants with embedded PSRAM include ESP32-S2FN4R2 and ESP32-S2R2.

[2] During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I2C are able to operate.

[3] The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When touch sensors work with a duty cycle of 1%, the typical current consumption is 22 μA.

4.5 Wi-Fi RF Characteristics

4.5.1 Wi-Fi RF Standards

Table 10: Wi-Fi RF Standards

Name		Description
Center frequency range of operating channel [1]		2412 ~ 2484 MHz
Wi-Fi wireless standard		IEEE 802.11b/g/n
Data rate	20 MHz	802.11b: 1, 2, 5.5 and 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n: MCS0-7, 72.2 Mbps (Max)
	40 MHz	802.11n: MCS0-7, 150 Mbps (Max)
Antenna type		PCB antenna, external antenna connector

[1] Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.

[2] For the modules that use external antenna connectors, the output impedance is 50 Ω. For other modules without external antenna connectors, the output impedance is irrelevant.

4.5.2 Transmitter Characteristics

Target TX power is configurable based on device or certification requirements. The default characteristics are provided in Table 11.

Table 11: TX Power Characteristics

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	19.5	—
802.11b, 11 Mbps	—	19.5	—
802.11g, 6 Mbps	—	18.0	—
802.11g, 54 Mbps	—	15.0	—
802.11n, HT20, MCS0	—	18.0	—
802.11n, HT20, MCS7	—	13.5	—
802.11n, HT40, MCS0	—	18.0	—
802.11n, HT40, MCS7	—	13.5	—

4.5.3 Receiver Characteristics

Table 12: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	–97	—
802.11b, 2 Mbps	—	–95	—
802.11b, 5.5 Mbps	—	–93	—
802.11b, 11 Mbps	—	–88	—
802.11g, 6 Mbps	—	–92	—
802.11g, 9 Mbps	—	–91	—
802.11g, 12 Mbps	—	–89	—
802.11g, 18 Mbps	—	–86	—
802.11g, 24 Mbps	—	–83	—
802.11g, 36 Mbps	—	–80	—
802.11g, 48 Mbps	—	–76	—
802.11g, 54 Mbps	—	–74	—
802.11n, HT20, MCS0	—	–92	—
802.11n, HT20, MCS1	—	–88	—
802.11n, HT20, MCS2	—	–85	—
802.11n, HT20, MCS3	—	–82	—
802.11n, HT20, MCS4	—	–79	—
802.11n, HT20, MCS5	—	–75	—
802.11n, HT20, MCS6	—	–73	—
802.11n, HT20, MCS7	—	–72	—
802.11n, HT40, MCS0	—	–89	—
802.11n, HT40, MCS1	—	–85	—
802.11n, HT40, MCS2	—	–83	—
802.11n, HT40, MCS3	—	–79	—
802.11n, HT40, MCS4	—	–76	—
802.11n, HT40, MCS5	—	–72	—

Cont'd on next page

Not Recommended For New Designs (NRND)

Table 12 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS6	—	–70	—
802.11n, HT40, MCS7	—	–68	—

Table 13: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 14: Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	14	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	13	—
802.11n, HT40, MCS0	—	19	—
802.11n, HT40, MCS7	—	8	—

5 Module Schematics

This is the reference design of the module.

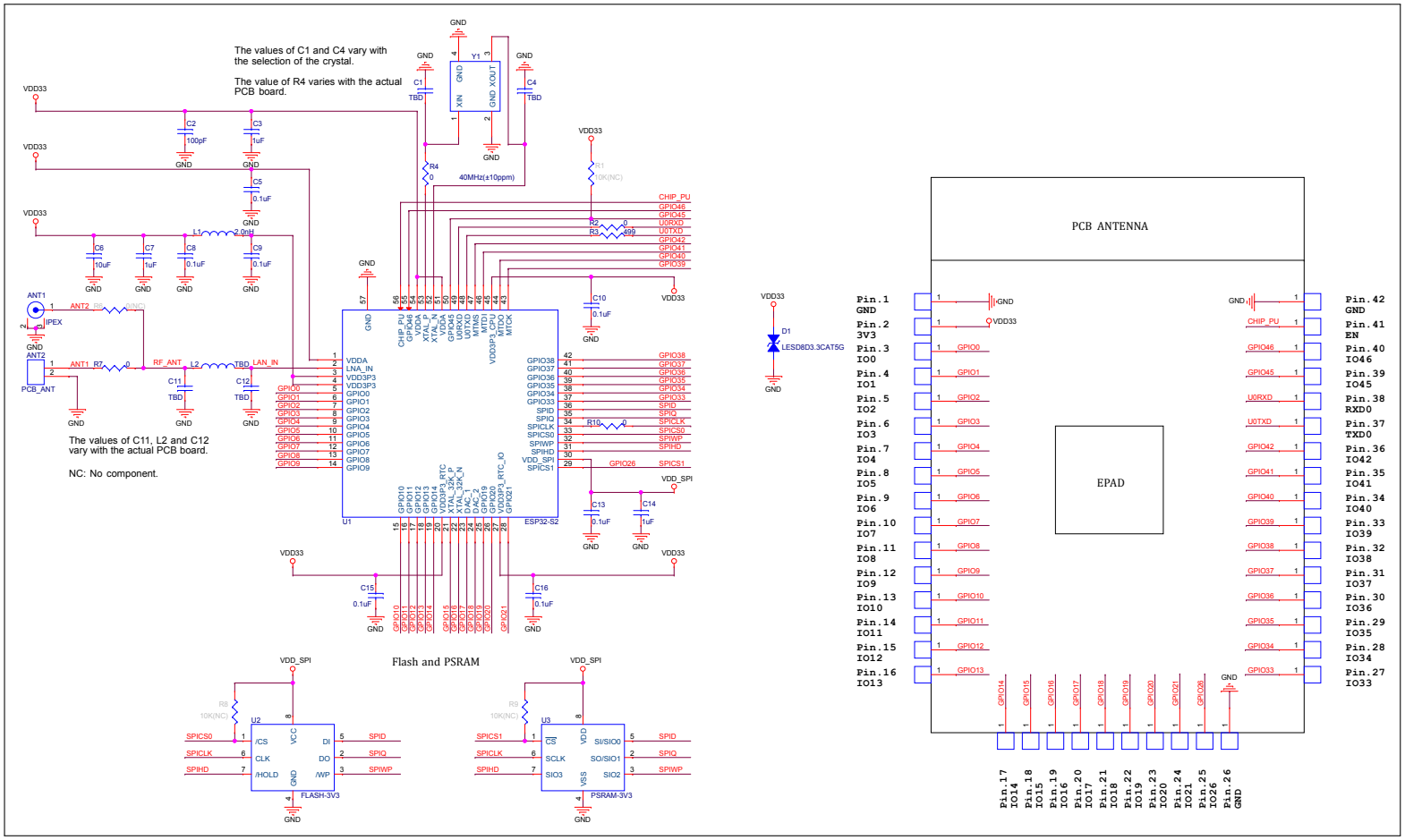

Figure 4: ESP32-S2-WROVER Schematics

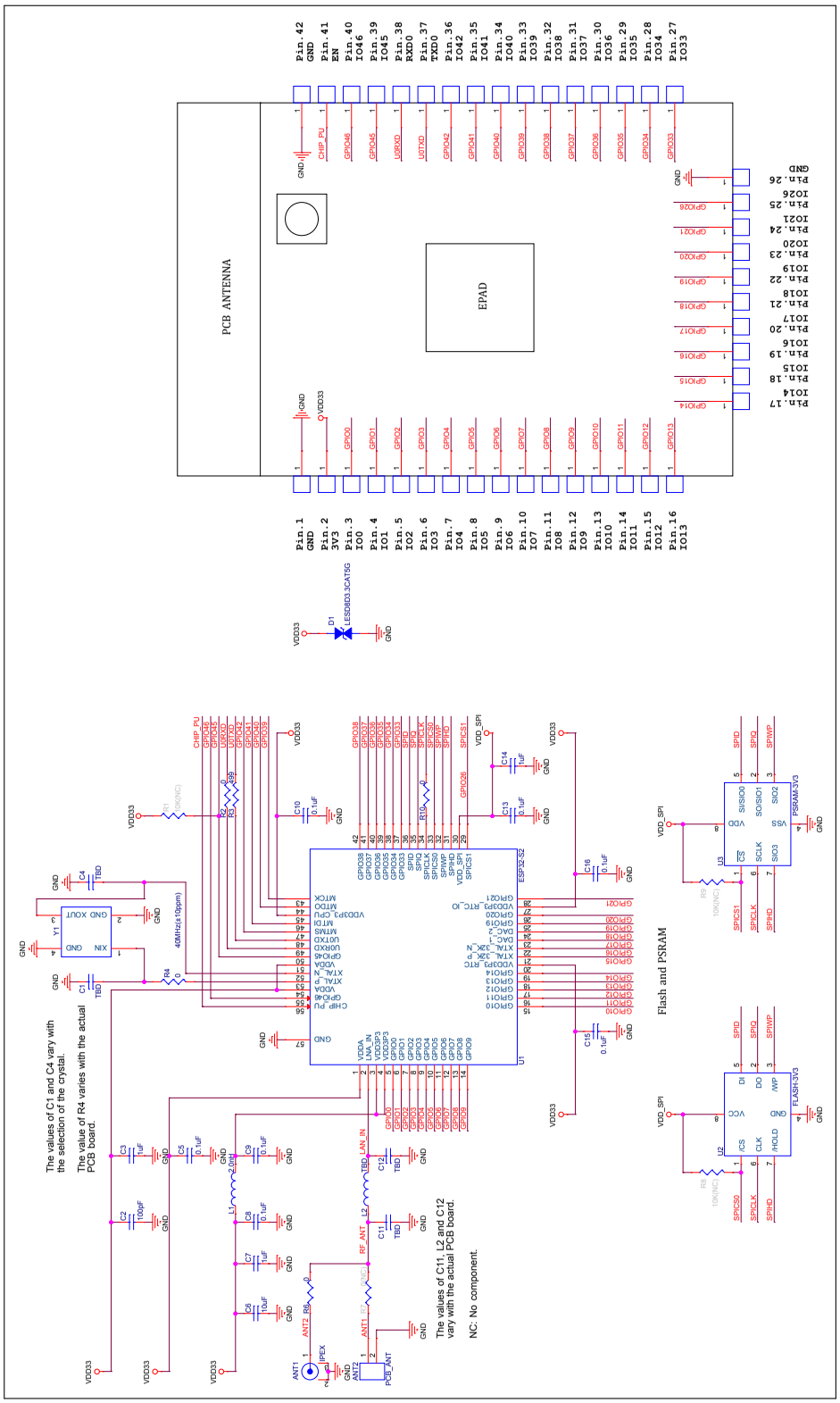

Figure 5: ESP32-S2-WROVER-I Schematics

6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

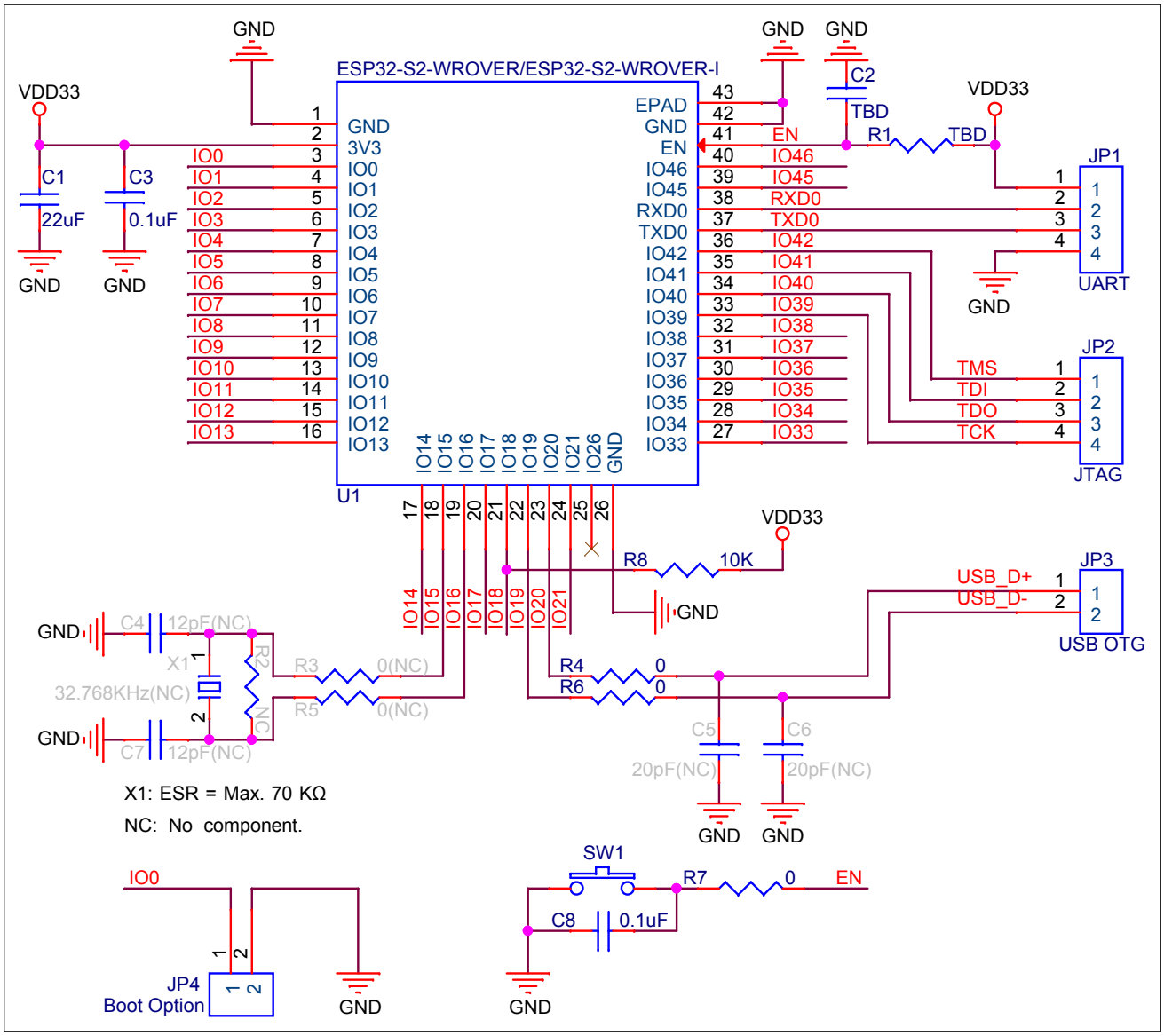

Figure 6: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste.
- To ensure that the power supply to the ESP32-S2 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S2's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32-S2 Series Datasheet*.
- GPIO18 works as U1RXD and is in floating state when the chip is powered on, which may affect the chip's entry into download boot mode. To solve this issue, add an external pull-up resistor.

7 Physical Dimensions and PCB Land Pattern

7.1 Physical Dimensions

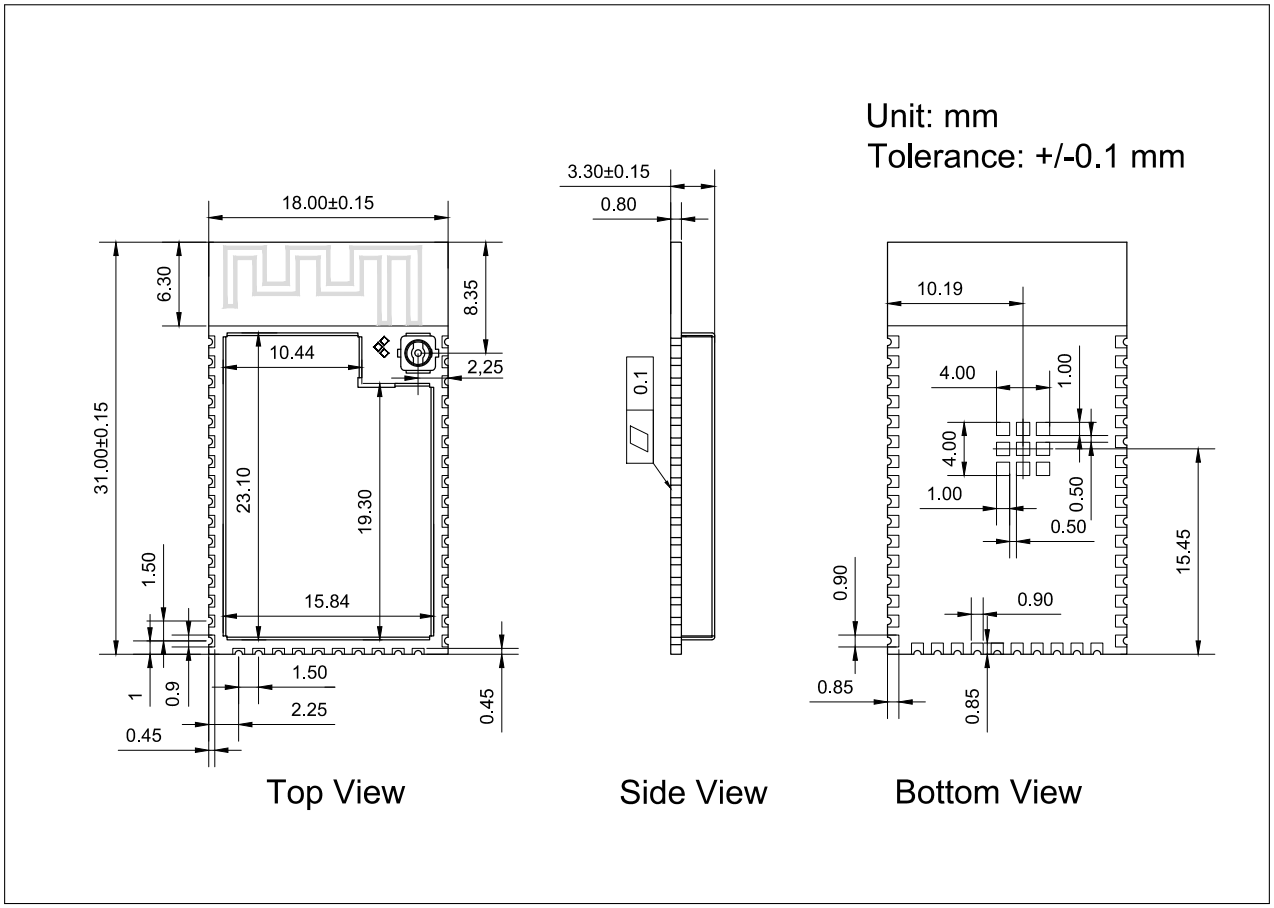

Figure 7: Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to *Espressif Module Package Information*.

7.2 Recommended PCB Land Pattern

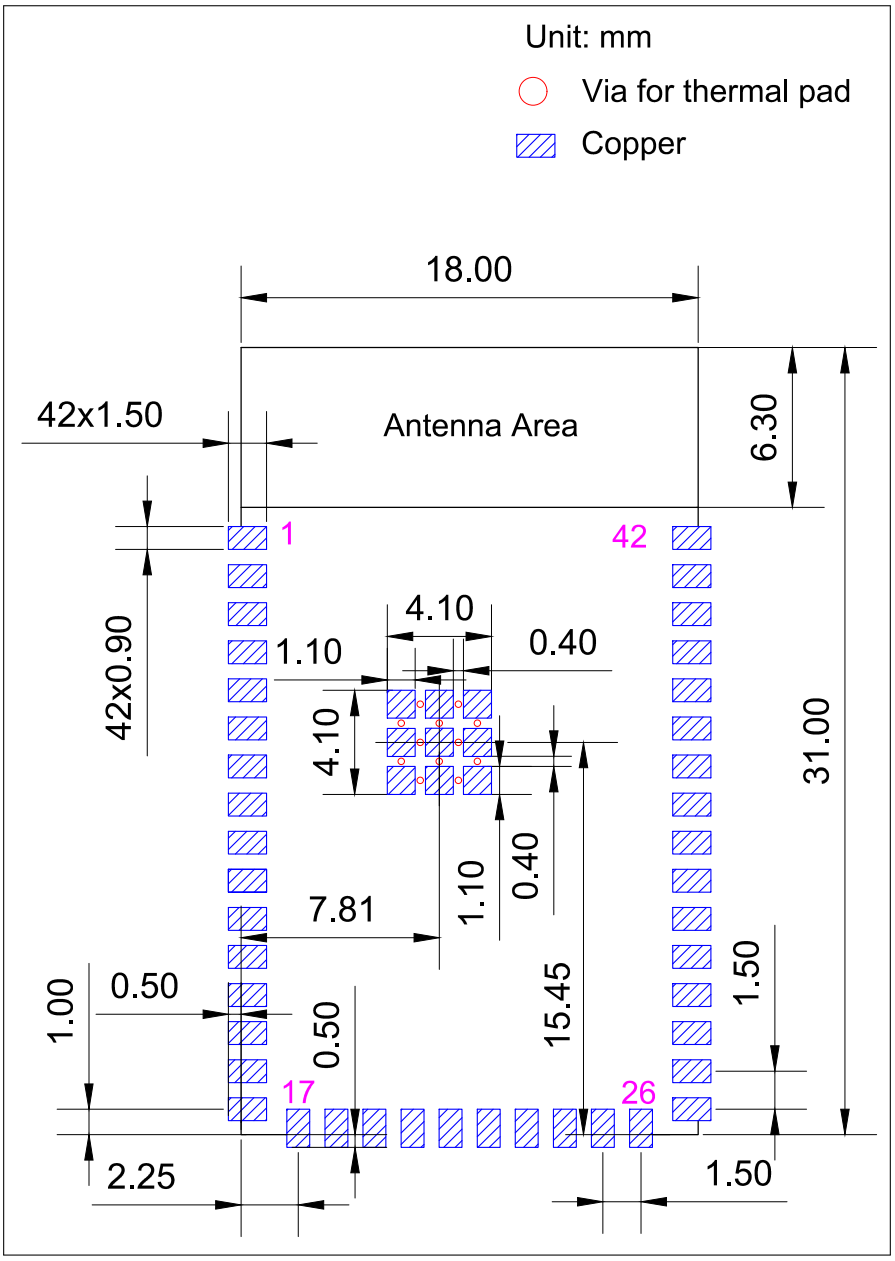

Figure 8: Recommended PCB Land Pattern

7.3 Dimensions of External Antenna Connector

ESP32-S2-WROVER-I uses the first generation external antenna connector as shown in Figure 9. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose
- MHF I connector from I-PEX
- AMC connector from Amphenol

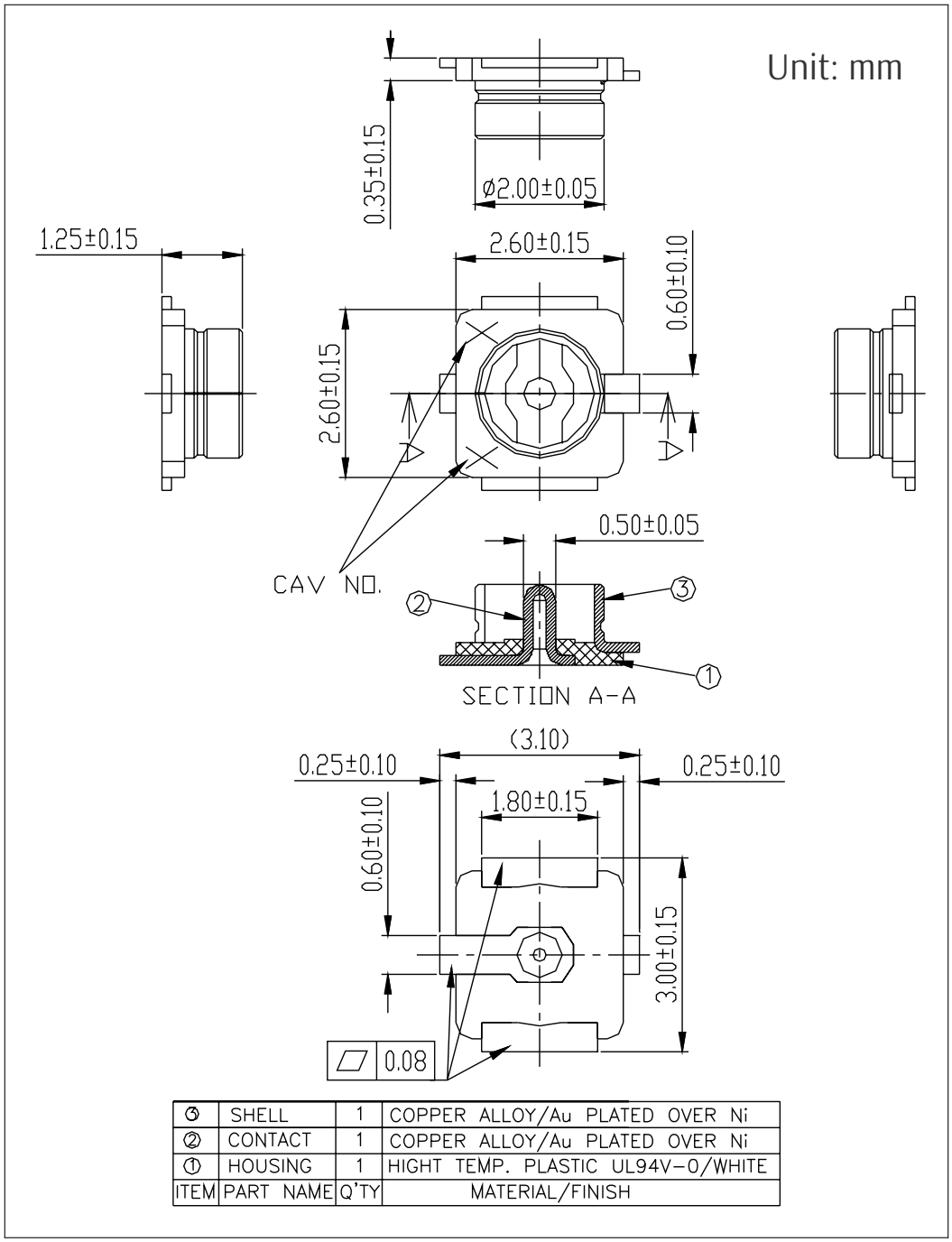

Figure 9: Dimensions of External Antenna Connector

8 Product Handling

8.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and /90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and /60%RH. If the above conditions are not met, the module needs to be baked.

8.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V
- Air discharge: ±6000 V
- Contact discharge: ±4000 V

8.3 Reflow Profile

Solder the module in a single reflow.

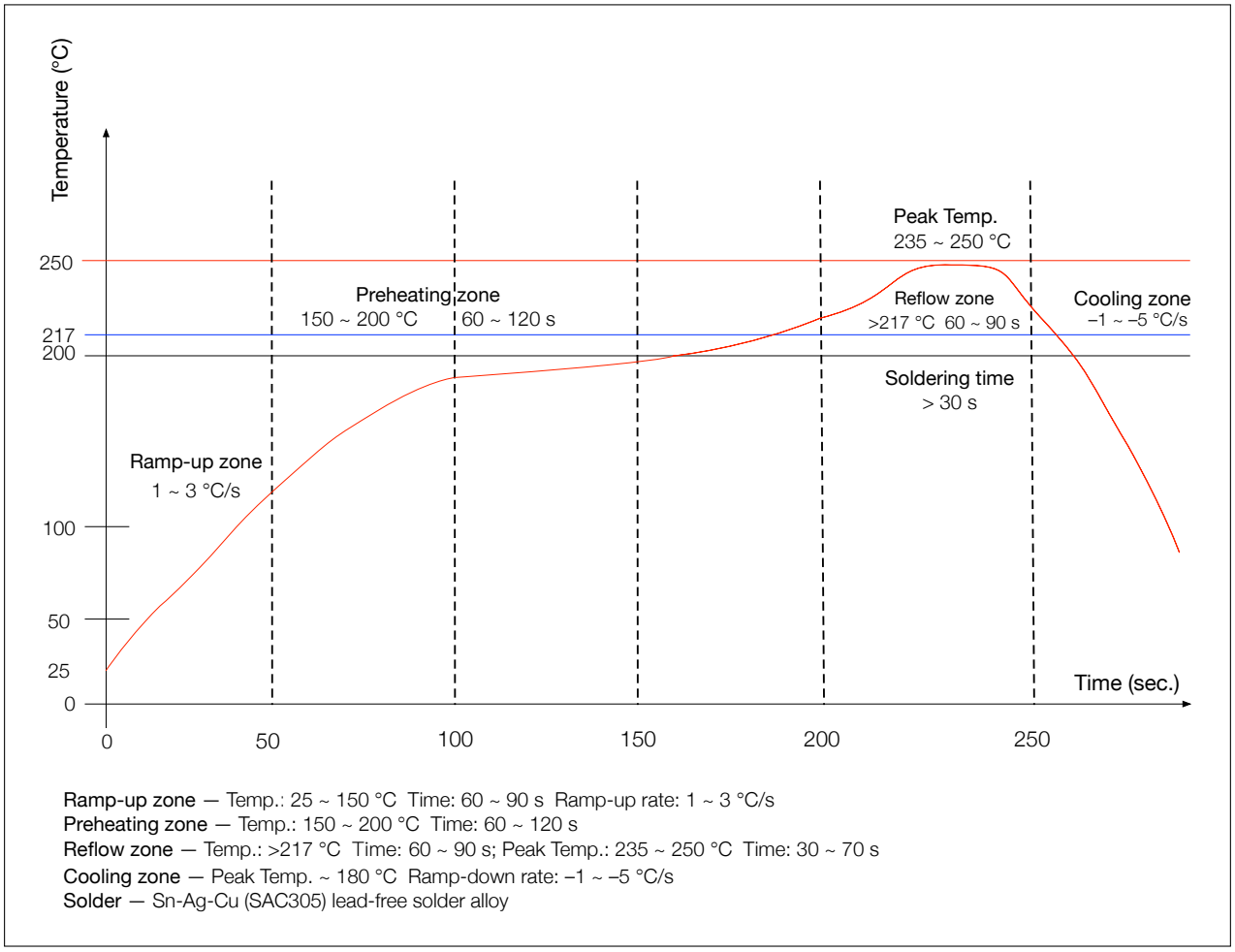

Figure 10: Reflow Profile

9 MAC Addresses and eFuse

The eFuse in ESP32-S2 family of chips has been burnt into 48-bit mac_address. The actual addresses the chip uses in station or AP modes correspond to mac_address in the following way:

- Station mode: mac_address
- AP mode: mac_address + 1

There are seven blocks in eFuse for users to use. Each block is 256 bits in size and has independent write/read disable controller. Six of them can be used to store encrypted key or user data, and the remaining one is only used to store user data.

10 Related Documentation and Resources

Related Documentation

- ESP32-S2 Series Datasheet – Specifications of the ESP32-S2 hardware.
- ESP32-S2 Technical Reference Manual – Detailed information on how to use the ESP32-S2 memory and peripherals.
- ESP32-S2 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S2 into your hardware product.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns
- *ESP32-S2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S2 Series SoCs* – Browse through all ESP32-S2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S2
- *ESP32-S2 Series Modules* – Browse through all ESP32-S2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S2
- *ESP32-S2 Series DevKits* – Browse through all ESP32-S2-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S2
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

Contact Us

- See the tabs *Sales Questions*, *Technical Enquiries*, *Circuit Schematic & PCB Design Review*, *Get Samples* (Online stores), *Become Our Supplier*, *Comments & Suggestions*.
  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2022-03-01	v1.2	• Added module introduction and pictures on the title page • Added NRND watermark • Added a note with a link and QR code to the latest version of the document • Updated Section "Learning Resources" and renamed to "Related Documentation and Resources" • Updated Table 8 and Table 9
2020-12-17	v1.1	• Added TWAI to Chapter 1 *Module Overview* • Updated Table 7 *Current Consumption Depending on RF Modes* • Updated the capacitance value of RC delay circuit to 1 μF in Chapter 6 *Peripheral Schematics* • Updated note in Section 8.3 *Reflow Profile*
2020-06-01	v1.0	Official release
2020-03-10	v0.5	Preliminary release

www.espressif.com

Disclaimer and Copyright Notice

Information in this document, including URL references, is subject to change without notice.

ALL THIRD PARTY'S INFORMATION IN THIS DOCUMENT IS PROVIDED AS IS WITH NO WARRANTIES TO ITS AUTHENTICITY AND ACCURACY.

NO WARRANTY IS PROVIDED TO THIS DOCUMENT FOR ITS MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, NOR DOES ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE.

All liability, including liability for infringement of any proprietary rights, relating to use of information in this document is disclaimed. No licenses express or implied, by estoppel or otherwise, to any intellectual property rights are granted herein.

The Wi-Fi Alliance Member logo is a trademark of the Wi-Fi Alliance. The Bluetooth logo is a registered trademark of Bluetooth SIG.

All trade names, trademarks and registered trademarks mentioned in this document are property of their respective owners, and are hereby acknowledged.

Not Recommended For New Designs (NRND)